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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,610	12/12/2003	Steven Frank	104853-0003	1959

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NUTTER MCCLENNEN & FISH LLP
WORLD TRADE CENTER WEST
155 SEAPORT BOULEVARD
BOSTON, MA 02210-2604

EXAMINER

PRICE, NATHAN E

ART UNIT	PAPER NUMBER
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2194

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/735,610

Applicant(s)

FRANK ET AL.

Examiner

Nathan Price

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-63 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-63 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.


Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.


WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to communications received 29 January 2007. Claims 1-63 are pending.

Response to Arguments

2. It does not appear that Applicant has responded to the issue raised regarding the Oath/Declaration.
3. Applicant's arguments filed 29 January 2007 regarding rejection of claims 36, 48 and 62 under 35 U.S.C. 112, 2nd paragraph, have been fully considered but they are not persuasive. The claims remain unclear as to whether the thread is delivered.
4. Applicant's arguments, see REMARKS and amended claims, filed 29 January 2007, with respect to claim objections and rejection of claims 17 – 27 under 35 U.S.C. 112, 2nd paragraph, have been fully considered and are persuasive. The objections of claims 1 - 51 and 57 - 63 have been withdrawn. The rejections of claims 17 – 27 under 35 U.S.C. 112, 2nd paragraph, have been withdrawn.
5. Applicant's arguments filed 29 January 2007 regarding rejections under 35 U.S.C. 103 have been fully considered but they are not persuasive.

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6. Applicant argues Jagannathan fails to teach delivering events without executing instructions and the handlers require instruction execution. However, Jagannathan teaches handlers execute in response to delivered events (col. 25 lines 22 – 26).

7. Applicant argues there is no motivation to combine the references. However, Brown focuses on details within the processor to provide increased instruction overlap [abstract] and Jagannathan discloses “highly parallel computer system” [abstract] that benefits from the increased overlap in execution. Both references teach the use of multiple physical processors (Fig. 1 of both references).

Oath/Declaration

8. The Oath/Declaration filed 26 April 2004 appears to indicate that no U.S. Application has been filed to which priority is claimed. However, the specification appears to contradict the Oath/Declaration by claiming the benefit of priority of Application Number 10/449,732. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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9. Claims 36, 48 and 62 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 36, 48 and 62 state, "to which the thread is delivered". It is not clear if the event or thread is being delivered. The claims will be treated as if they state, "processing the event by the thread to which the event is delivered" for the remainder of the Office Action. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 1 – 3, 5 – 14, 16 – 23, 27 – 37, 39 – 52 and 56 – 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown, III et al (US 6,240,508 B1; hereinafter Brown) in view of Jagannathan et al (US Pat. 5,692,193; hereinafter Jagannathan).

As to claim 1, Brown teaches an embedded processor, comprising

a plurality of processing units [Fig. 1, CPUs 10, 28; col. 7 lines 24 –

48],

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one or more execution units that are shared by, and in communication coupling with, the plurality of processing units, the execution units executing instructions from the threads [Fig. 1, CPUs 10, 28; col. 7 lines 24 – 48], and

an event delivery mechanism that delivers events [col. 14 lines 1 – 17].

Even though Brown teaches multiple CPUs, Brown fails to specifically teach multiple threads. However, Jagannathan teaches each processing unit executing one or more processes or threads (which one or more processes or threads are collectively referred to as “threads”) [abstract; Fig. 1 threads 18 and processors 12] and an event delivery mechanism that delivers events to respective threads with which those events are associated, wherein the event deliver mechanism is in communication coupling with the plurality of processing units, and delivers each such event to the respective thread without execution of instructions by said processing units [col. 22 lines 53 – 59; col. 24 lines 1 – 62]. It would have been obvious to one of ordinary skill in the art at the time Applicant’s invention was made to combine these references because Brown focuses on details within the processor to provide increased instruction overlap [abstract] and Jagannathan discloses “highly parallel computer system” [abstract] that benefits from the increased overlap in execution.

As to claims 2, 3, 5 and 6, the combination of Brown (B) and Jagannathan (J) teaches:

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[claim 2] that the thread to which an event is delivered processes that event without execution of instructions outside that thread [J: col. 24 lines 9 – 29, 51 – 62],

[claim 3] that the events include any of hardware interrupts, software-initiated signaling events (“software events”) and memory events [J: col. 19 lines 9 – 25; col. 22 lines 53 – 59; col. 24 lines 50 – 62],

[claim 5] that each thread is any of constrained or not constrained to execute on a same processing unit during a life of that thread [J: col. 6 lines 3 – 41], and

[claim 6] that at least one of the processing units is a virtual processing unit [J: abstract, Fig. 1 virtual processors 16].

As to claim 7, the combination of Brown (B) and Jagannathan (J) teaches a pipeline control that is in communication coupling with the plurality of processing units and with the plurality of execution units, the pipeline control launching instructions from plural ones of the threads for concurrent execution on plural ones of the execution units [B: Fig. 1 CPUs 10 and 28, I-BOX 17, E-BOX 23, F-BOX 27; col. 5 lines 27 – 43; col. 7 lines 24 – 48]. See the rejections of claims 1 – 3 and 5 for limitations not specifically addressed.

As to claims 8 – 14 and 16, the combination of Brown (B) and Jagannathan (J) teaches:

[claim 8] the pipeline control comprises a plurality of instruction queues [B: col. 4 line 66 – col. 5 line 7], each associated with a respective virtual processing unit [J: col. 3 lines 59 – 67; col. 9 lines 45 – 60] (Brown fails to specifically teach

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virtual processing units, but it is taught by Jagannathan, see the rejection of claim 6),

[claim 9] the pipeline control decodes instruction classes from the instruction queues [B: col. 5 lines 14 – 43; col. 7 lines 24 – 30],

[claim 10] the pipeline control controls access by the processing units to a resource providing source and destination registers for the instructions dispatched from the instruction queues [B: col. 14 lines 33 – 60; col. 15 lines 15 – 35],

[claim 11] the execution units include a branch execution unit responsible for any of instruction address generation, address translation and instruction fetching [B: col. 13 lines 53 – 67],

[claim 12] the branch execution unit maintains state for the virtual processing units [B: col. 13 lines 53 – 67],

[claim 13] the pipeline control controls access by the virtual processing units to the execution units [B: col. 12 lines 18 – 38; col. 14 lines 1 – 17] [J: col. 3 lines 59 – 67; col. 9 lines 5 – 19] (Brown fails to specifically teach virtual processing units, but it is taught by Jagannathan, see rejection of claim 6),

[claim 14] the pipeline control signals a branch execution unit that is shared by the virtual processing unit as the instruction queue for each virtual processing unit is emptied [B: col. 13 lines 53 – 67] [J: col. 3 lines 59 – 67] (Brown fails to specifically teach virtual processing units, but it is taught by Jagannathan, see rejection of claim 6), and

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[claim 16] the plurality of execution units include any of integer, floating, branch, compare and memory units [B: col. 5 lines 14 – 27; col. 7 lines 24 – 48; col. 10 lines 11 – 17].

As to claims 17 – 22, see the rejections of claims 1 – 3, 5, 7, 11, 12, 14 and 16. With respect to the plurality of embedded processors, both Brown and Jagannathan disclose multiple physical processors (Figure 1 of both documents). This is also applied to the rejections of other claims that recite a plurality of embedded processors that refer to the rejection of claim 1.

As to claim 23, the combination of Brown (B) and Jagannathan (J) teaches instructions fetched by the branch execution unit are placed in the instruction queues associated with the respective virtual processing unit in which the corresponding thread is executed [B: col. 13 lines 53 – 67] [J: col. 3 lines 59 – 67]. Brown fails to specifically teach virtual processing units, but it is taught by Jagannathan, see rejection of claim 6. See the rejections of claims 7 and 8 for limitations not specifically addressed.

As to claim 27, the combination of Brown (B) and Jagannathan (J) teaches the pipeline control launches, and the execution units execute, multiple instructions from one or more threads simultaneously [B: col. 8 lines 23 – 51; col. 22 lines 19 – 51] [J: col. 3 lines 13 – 25, 59 – 67] (Brown fails to specifically teach threads, but it is taught by Jagannathan, see rejection of claim 6).

As to claims 28 – 31, see the rejections of claims 1 – 3, 5 and 6.

As to claims 32 – 34, see the rejections of claims 17 – 19.

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As to claims 35 – 37, 39 and 40, see the rejections of claims 1 – 3, 5 and 6.

As to claims 41 – 46, see the rejections of claims 7, 9, 10, 11, 12, 14 and 16.

As to claims 47 – 51, see the rejections of claims 17 – 21.

As to claims 52 and 56, see the rejections of claims 23 and 27.

As to claims 57 – 60, see the rejections of claims 1, 2, 3, 5 and 6.

As to claims 61 – 63, see the rejections of claims 1, 2, 3, 5 and 6.

11. Claims 4, 24 – 26, 38 and 53 – 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown in view of Jagannathan as applied to claims 1, 23, 35 and 52 above, and further in view of Eggers (Eggers et al. "Simultaneous Multithreading: A Platform for Next-Generation Processors," IEEE, 1997; pages 12 – 19.).

As to claims 4 and 38, Brown and Jagannathan fail to specifically teach executing instructions without knowing which thread they are from. However, Eggers teaches that the execution units execute instructions from the threads without need to know what thread they are from [page 13, right column, ¶ 3]. It would have been obvious to one of ordinary skill in the art at the time Applicants invention was made to combine these references because Eggers discloses parallel execution techniques [page 12, left column ¶ 2] to further increase execution overlap, which is a goal of Brown [abstract].

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As to claims 24 and 53, Brown fails to specifically teach keeping the instruction queues at equal levels. However, Eggers teaches one or more instructions are fetched at a time for a thread with a goal of keeping the instruction queues at equal levels [page 14, right column, ¶ 3 and 4]. See the rejection of claims 4 and 38 for motivation to combine.

As to claims 25 and 54, Brown teaches the pipeline control dispatches one or more instructions at a time from a given instruction queue for execution [col. 14 lines 1 – 17].

As to claims 26 and 55, Brown teaches a number of instructions dispatched by the pipeline control at a given time from a given instruction queue is controlled by a stop flag in a sequence of instructions in that queue [col. 13 line 53 – col. 14 line 17].

12. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brown in view of Jagannathan as applied to claim 7 above, and further in view of Gosior et al (US 2003/0120896 A1; hereinafter Gosior). Brown fails to specifically teach reducing power consumption. However, Gosior teaches the pipeline control idles the execution units to decrease power consumption [¶ 31]. It would have been obvious to one of ordinary skill in the art at the time Applicant's invention was made to combine these references because Gosior teaches a multithreaded pipeline processor that controls use of resources and power management that can provide the advantage of reduced power

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consumption [¶ 22, 31] during the operation of the system disclosed by Brown [col. 25 lines 29 – 35].

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan Price whose telephone number is (571) 272-4196. The examiner can normally be reached on 6:30am - 3:00pm, Monday - Friday.

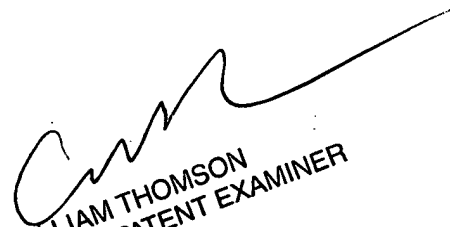
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Thomson can be reached on (571) 272-3718.

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The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NP


WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER